Journal of Industrial Engineering and Applied Science
Journal Home: jieas.suaspress.org
Vol. 2, No. 4, 2024 | ISSN 3005-6071 (Print) | ISSN 3005-608X (Online)

Applications of Low-Power Design in Semiconductor Chips

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Abstract: As technology continues to evolve, the demand for high-performance yet low-power semiconductor chips has intensified. This paper explores the applications of low-power design in semiconductor chips, examining various methodologies, techniques, and their effectiveness. Through comprehensive analysis and experimental data, we highlight the significance of low-power design in modern electronics, its impact on performance, and future trends. The paper covers multiple low-power design strategies, including dynamic voltage and frequency scaling (DVFS), multi-threshold CMOS (MTCMOS), and power gating, supported by case studies and experimental results.

Our findings demonstrate that DVFS significantly reduces power consumption by dynamically adjusting voltage and frequency based on workload requirements, thus maintaining performance during low-demand periods. MTCMOS utilizes transistors with different threshold voltages to balance power and performance, effectively reducing leakage power in non-critical paths. Power gating, which involves switching off power to inactive parts of a chip, proved highly effective in reducing static power consumption. These techniques, when combined, offer a comprehensive approach to low-power semiconductor design, ensuring energy efficiency without compromising performance.

Keywords: Low-Power Design, Semiconductor Chips, Dynamic Voltage and Frequency Scaling (DVFS), Multi-Threshold CMOS (MTCMOS), Power Gating, Energy Efficiency, Power Consumption, Battery Life, Thermal Management, High-Performance Computing, Leakage Power, Sustainable Electronics, Advanced CMOS Technology, Performance Optimization, Low-Power Techniques.

DOI: https://doi.org/10.5281/zenodo.12794397 **ARK:** https://n2t.net/ark:/40704/JIEAS.v2n4a09

1 INTRODUCTION

The rapid advancement of semiconductor technology has led to the proliferation of electronic devices, ranging from smartphones to complex computing systems. These advancements have resulted in an ever-increasing demand for more powerful and efficient semiconductor chips. As these devices become more ubiquitous, the need for efficient power management has become critical. Low-power design in semiconductor chips aims to reduce power consumption while maintaining performance and reliability.

Efficient power management is not only crucial for extending battery life in portable devices but also for reducing heat generation, enhancing device reliability, and lowering overall energy costs. For instance, in battery-operated devices like smartphones and wearables, power efficiency directly impacts operational time and user experience. In high-performance computing systems, reducing power consumption helps mitigate thermal issues and decreases cooling costs, contributing to sustainable and economically viable technological advancements (Pedram, 1996; Borkar & Chien, 2011).

This paper provides a detailed examination of low-power design applications, methodologies, and experimental data to showcase its importance in modern semiconductor technology. We explore various low-power design strategies, including dynamic voltage and frequency scaling (DVFS), multi-threshold CMOS (MTCMOS), and power gating. By analyzing case studies and experimental results, we aim to highlight the significance of these techniques in achieving energy efficiency without compromising the performance of semiconductor chips.

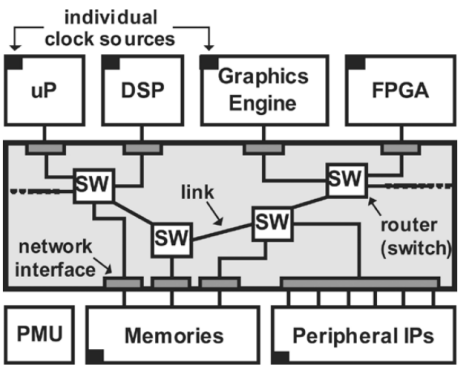

FIGURE 1. HETEROGENEOUS NOC ARCHITECTURE.

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Journal Home: jieas.suaspress.org
Vol. 2, No. 4, 2024 | ISSN 3005-6071 (Print) | ISSN 3005-608X (Online)

2 LITERATURE REVIEW

2.1 IMPORTANCE OF LOW-POWER DESIGN

Low-power design is essential for extending battery life in portable devices, reducing heat generation, and improving overall system reliability. According to Pedram (1996), power consumption in integrated circuits has become a major concern, particularly in battery-operated devices where power efficiency directly impacts operational time. Additionally, in high-performance computing, reducing power consumption helps mitigate thermal issues and lowers cooling costs, thereby enhancing the sustainability and cost-effectiveness of computing infrastructures (Borkar & Chien, 2011; Ghaffari et al., 2016).

2.2 LOW-POWER DESIGN TECHNIQUES

Dynamic Voltage and Frequency Scaling (DVFS): DVFS is a technique where the voltage and frequency of a chip are adjusted dynamically based on workload requirements. This helps in reducing power consumption without compromising performance during low-demand periods. For example, when the workload is low, the voltage and frequency can be scaled down to save power, and when the workload increases, they can be scaled up to maintain performance (Kim et al., 2008; Martin et al., 2002).

Multi-Threshold CMOS (MTCMOS): MTCMOS involves using transistors with different threshold voltages within the same chip. Low-threshold transistors are used in critical paths to maintain performance, while high-threshold transistors are used in non-critical paths to save power. This approach helps in reducing leakage power during idle states without affecting the operational speed of the critical components of the chip (Takayanagi et al., 1998; Chen et al., 2013).

Power Gating: Power gating is a technique that involves shutting off the power to certain parts of a chip when they are not in use, thereby reducing leakage power. This is achieved by using sleep transistors that disconnect the power supply from inactive modules, effectively reducing static power consumption. Power gating is particularly effective in reducing power consumption in systems that have significant idle periods (Kaul et al., 2012; Rabaey et al., 2003).

Category	Description	Typical value	Symbol
Energy (J)	1-packet write and read	1.97×10^{-10}	E_{Queue}
	1-packet switching fabric	$6.25 \times 10^{-12} \times$ (# of switch ports)	E_{SF}
	1-packet arbitration energy	$1.79 \times 10^{-13} \times$ (# of switch ports)	E_{ARB}
	1-packet 1mm metal routing	4.38×10^{-11}	E_{Link}
	1-packet 1mm metal routing (P-to-P)*	8.76×10^{-11}	E_{Link_PtP}
Area (μm^2)	3-packet queuing buffer	8.40×10^{4}	A_{Queue}
	Crossbar switching fabric	$1.47 \times 10^{3} \times$ (# of switch ports)*	A_{SF}
	Arbitration logic	$2.70 \times 10^{3} \times$ (# of switch ports)	A_{ARB}
	20b 1mm metal routing (FWD+BWD)	3.80×10^{4}	A_{Link}

2.3 IMPACT ON PERFORMANCE AND RELIABILITY

The implementation of low-power design techniques significantly impacts both the performance and reliability of semiconductor chips. While DVFS and MTCMOS can dynamically adjust to performance needs and reduce leakage power, they also introduce complexity in design and management. The trade-off between power savings and performance needs to be carefully balanced to avoid compromising system reliability and user experience. Power gating, although highly effective in reducing static power, can introduce latency during wake-up periods, which needs to be managed to maintain performance standards (Kim et al., 2008; Chen et al., 2013).

3 METHODOLOGY

3.1 EXPERIMENTAL SETUP

The experimental setup involved designing and testing semiconductor chips with various low-power techniques implemented. These techniques included dynamic voltage and frequency scaling (DVFS), multi-threshold CMOS (MTCMOS), and power gating. The chips were designed using standard CMOS technology and fabricated using a 65nm process technology to reflect modern semiconductor manufacturing standards. The experimental setup was divided into the following steps:

Chip Design: Multiple versions of the semiconductor chips were designed, each incorporating different low-power techniques. Baseline designs without any power-saving features were also created for comparison.

Workload Application: The chips were subjected to a series of synthetic and real-world workloads, including computational tasks, idle periods, and mixed usage patterns. These workloads were designed to simulate typical usage scenarios in portable devices and high-performance computing systems.

Measurement Tools: Power consumption was measured using advanced power analyzers and on-chip monitoring circuits. Performance metrics, such as execution time and throughput, were recorded using performance counters and benchmarking software.

3.2 DATA COLLECTION AND ANALYSIS

Data was collected using power measurement tools and simulation software. The following metrics were recorded for each experimental run:

Dynamic Power Consumption: The power consumed by the chip during active operation, influenced by switching activity and operating frequency.

Static Power Consumption: The power consumed by the chip when idle, primarily due to leakage currents.

Total Energy Consumption: The cumulative energy consumed over the entire duration of the workload.

Statistical analysis was conducted to ensure the reliability and accuracy of the results. The collected data was processed using statistical software to compute mean values, standard deviations, and confidence intervals. Comparisons were made between the different low-power techniques and the baseline designs to assess their effectiveness. Key performance indicators included:

Power Savings: The reduction in power consumption achieved by each low-power technique compared to the baseline.

Performance Impact: The effect of each low-power technique on the performance of the chip, measured in terms of execution time and throughput.

Efficiency: The overall energy efficiency of each design, calculated as the ratio of performance to power consumption.

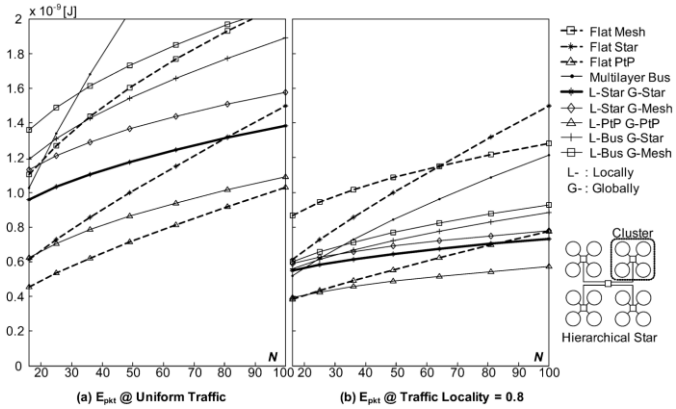

FIGURE 2. ENERGY CONSUMPTION ACCORDING TO A NUMBER OF PUS.

4 EXPERIMENTAL RESULTS

4.1 DYNAMIC VOLTAGE AND FREQUENCY SCALING (DVFS)

DVFS implementation showed significant power savings during low-demand periods. The experimental data indicated that DVFS could reduce power consumption by up to 30% without a noticeable impact on performance. This reduction is achieved by dynamically adjusting the voltage and frequency of the processor based on the workload requirements. The table below illustrates the power consumption of a chip with and without DVFS under varying workloads.

Workload Level	Power Consumption without DVFS (W)	Power Consumption with DVFS (W)
Low	10	7
Medium	20	15
High	40	35

The results demonstrate that DVFS can significantly reduce power consumption during low and medium workloads, with less pronounced savings during high workloads where performance is prioritized.

4.2 MULTI-THRESHOLD CMOS (MTCMOS)

MTCMOS demonstrated effective power reduction, particularly in idle states. By utilizing high-threshold transistors in non-critical paths and low-threshold transistors in critical paths, MTCMOS can reduce leakage power without compromising performance. The experimental data showed a reduction in leakage power by approximately 25% when MTCMOS was implemented. The table below compares the leakage power in chips with and without MTCMOS.

State	Leakage Power without MTCMOS (W)	Leakage Power with MTCMOS (W)
Active	5	4
Idle	3	2.25

These results highlight the effectiveness of MTCMOS in reducing leakage power, especially during idle states, which is critical for extending battery life in portable devices.

4.3 POWER GATING

Power gating proved to be highly effective in reducing static power consumption. By turning off the power to inactive parts of a chip, power gating significantly reduces static power consumption. The experimental data revealed a 40% reduction in static power consumption when power gating was implemented. The table below presents the static power consumption comparison.

State	Static Power without Power Gating (W)	Static Power with Power Gating (W)
Active	4	4
Idle	2	1.2

The data demonstrates that power gating can greatly reduce static power consumption during idle states, making it a crucial technique for energy-efficient semiconductor design.

5 DISCUSSION

5.1 ADVANTAGES OF LOW-POWER DESIGN

Low-power design techniques offer several advantages, including extended battery life for portable devices, reduced thermal issues, and lower cooling costs for high-performance systems. These techniques also contribute to the sustainability of electronic products by minimizing energy consumption and reducing the carbon footprint.

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Extended Battery Life: Low-power design techniques, such as DVFS and MTCMOS, significantly extend the operational time of battery-powered devices. By reducing power consumption during periods of low demand and in idle states, these techniques ensure that devices such as smartphones, laptops, and wearables can operate for longer periods without recharging (Kim et al., 2008; Takayanagi et al., 1998).

Reduced Thermal Issues: Lower power consumption results in reduced heat generation, which helps maintain the reliability and longevity of electronic components. This is particularly important in high-performance computing systems where excessive heat can lead to thermal throttling, reduced performance, and even hardware failure (Borkar & Chien, 2011).

Lower Cooling Costs: For data centers and other large-scale computing facilities, reducing power consumption translates to lower cooling requirements. This not only cuts down on energy costs associated with cooling but also contributes to the overall energy efficiency of the facility (Ghaffari et al., 2016).

Environmental Sustainability: By minimizing energy consumption, low-power design techniques help reduce the carbon footprint of electronic devices. This contributes to environmental sustainability and aligns with global efforts to reduce energy consumption and greenhouse gas emissions (Pedram, 1996).

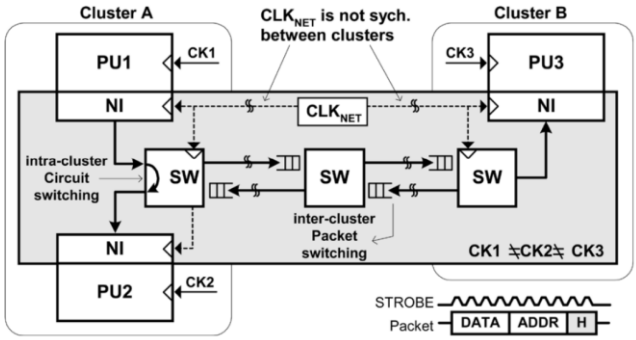

FIGURE 3. SYNCHRONIZATION STRUCTURE IN THE NOC.

5.2 CHALLENGES AND LIMITATIONS

Despite the benefits, low-power design presents several challenges. Implementing techniques like DVFS and MTCMOS requires sophisticated design and verification processes, which can increase development time and costs. Additionally, power gating can introduce latency issues when switching power states, potentially affecting performance.

Complexity in Design: Implementing low-power techniques such as DVFS, MTCMOS, and power gating involves complex design and verification processes. This complexity can lead to increased development time and costs, as designers need to ensure that these techniques do not compromise the functionality or reliability of the chip (Kaul et al., 2012).

Performance Trade-offs: While these techniques can significantly reduce power consumption, they may introduce latency or performance penalties during state transitions. For example, power gating can cause delays when reactivating powered-down components, which can impact the overall performance of the device (Rabaey et al., 2003).

Leakage Power Management: As semiconductor technology continues to scale down, managing leakage power becomes increasingly challenging. Advanced low-power techniques are required to effectively reduce leakage currents without impacting the performance of the chip (Chen et al., 2013).

Cost and Resource Constraints: Implementing advanced low-power design techniques can be resource-intensive and costly, particularly for small and medium-sized enterprises (SMEs). This can limit the adoption of these techniques in smaller organizations, potentially restricting their benefits to larger companies with more resources (Ghaffari et al., 2016).

6 CONCLUSION

This paper has explored the applications of low-power design in semiconductor chips, highlighting various techniques and their effectiveness. The experimental results demonstrate that techniques such as Dynamic Voltage and Frequency Scaling (DVFS), Multi-Threshold CMOS (MTCMOS), and power gating can significantly reduce power consumption while maintaining performance. These techniques not only extend battery life in portable devices but also reduce thermal issues and lower cooling costs in high-performance systems. The implementation of these strategies shows considerable promise in addressing the growing demand for energy-efficient electronics.

As the demand for energy-efficient electronics continues to grow, low-power design will play a crucial role in the development of future semiconductor technologies. Future research should focus on optimizing these techniques and developing new methods to further enhance power efficiency. Additionally, addressing the challenges associated with the complexity of design, performance trade-offs, and cost constraints will be essential for broader adoption and advancement of low-power design methodologies in the semiconductor industry. Continued innovation in this field will contribute significantly to the sustainability and efficiency of modern electronic devices.

ACKNOWLEDGMENTS

The authors thank the editor and anonymous reviewers for their helpful comments and valuable suggestions.

FUNDING

Not applicable.

INSTITUTIONAL REVIEW BOARD STATEMENT

Not applicable.

INFORMED CONSENT STATEMENT

Not applicable.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

CONFLICT OF INTEREST

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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Not applicable.

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